Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **GAIN**
2. **INPUT-**
3. **INPUT+**
4. **GND**
5. **V OUT**
6. **VS**
7. **BYPASS**
8. **GAIN**

**.050”**

**.050”**

**L**

**M**

**3**

**8**

**6**

**MASK**

**REF**

**4 3**

**2**

**1**

**6 7 8**

**4**

**5**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” X .003” min.**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .050” X .050” DATE: 11/11/21**

**MFG: NATIONAL THICKNESS .011” P/N: LM386**

**DG 10.1.2**

#### Rev B, 7/1